



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

118

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,892	01/21/2004	Tien-Jen Cheng	FIS920030352US1	1891
32074 7590 02/01/2007 INTERNATIONAL BUSINESS MACHINES CORPORATION DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533			EXAMINER LANDAU, MATTHEW C	
			ART UNIT	PAPER NUMBER
			2815	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		02/01/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.		Applicant(s)	
	10/707,892		CHENG ET AL.	
	Examiner		Art Unit	
	Matthew Landau		2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,7-14 and 21-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5,7-14 and 21-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7, and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (US PGPub 2005/0103636, hereinafter Cheng).

The applied reference has a common assignee/inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1, 5, and 7, Figure 6 of Cheng discloses a terminal metal layer 106/102 disposed on a passivating layer 108/110; a diffusion barrier layer (116 and the CrCu portion of 118) on said terminal metal layer; a conducting layer pad (Cu portion of 118) on said diffusion barrier; a hard test barrier layer (Ni) 122 (paragraph [0014]) on, and enclosing, said conducting layer pad; and a plate passivating layer (Au) 124 (paragraph [0014]) on said hard test barrier. Note that Cheng discloses layer 118 can be a multi-layered structure of Cu/CrCu (paragraph

Art Unit: 2815

[0013]). Therefore, the Cu layer is considered to be the conducting layer pad, and the CrCu layer is considered to be part of the diffusion layer.

Regarding claims 2-4 and 22-24, Figure 6 of Cheng discloses said diffusion barrier layer includes an adhesion layer (CrCu portion of 118) on barrier metallurgy (TiW) 116 (paragraph [0013]).

Regarding claims 21 and 25, Figure 6 of Cheng discloses a terminal metal layer 106/102 disposed on a passivating layer 108/110; a diffusion barrier layer (116 and the CrCu portion of 118) on said terminal metal layer; a copper seed layer pad (Cu portion of 118) on said diffusion barrier; a nickel layer 122 (paragraph [0014]) plated to, and enclosing, said copper seed layer pad; and a plate passivating layer (Au) 124 (paragraph [0014]) on said nickel layer. Note that Cheng discloses layer 118 can be a multi-layered structure of Cu/CrCu (paragraph [0013]). Therefore, the Cu layer is considered to be the copper seed layer pad, and the CrCu layer is considered to be part of the diffusion layer.

Claims 1, 2, 5, 7, 21, 22, and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Biggs et al. (US PGPub 2005/0062170, hereinafter Biggs).

The applied reference has a common assignee/inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived

Art Unit: 2815

from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1, 5, and 7, Figure 6 of Biggs discloses a terminal metal layer 16/18 disposed on a passivating layer 12/14; a diffusion barrier layer 36 on said terminal metal layer; a conducting layer pad 38 on said diffusion barrier; a hard test barrier layer (Ni) 48 (paragraph [0012]) on, and enclosing, said conducting layer pad; and a plate passivating layer (Au) 50 (paragraph [0012]) on said hard test barrier.

Regarding claims 2 and 22, Biggs discloses layer 36 consists of a layer of Ta and a layer of TaN (paragraph [0008]). The Ta layer can be considered the adhesion layer and the TaN layer can be considered the barrier metallurgy.

Regarding claims 21 and 25, Figure 6 of Biggs discloses a terminal metal layer 16/18 disposed on a passivating layer 12/14; a diffusion barrier layer 36 on said terminal metal layer; a copper seed layer pad 38 on said diffusion barrier; a nickel layer 48 (paragraph [0012]) plated to, and enclosing, said copper seed layer pad; and a plate passivating layer (Au) 50 (paragraph [0012]) on said nickel layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2815

Claims 8-13 are rejected under 35 U.S.C. 102(e) as anticipated by Cheng or, in the alternative, under 35 U.S.C. 103(a) as obvious over Cheng in view of McCormick (US Pat. 6,706,622).

Regarding claims 8 and 11-13, Figure 6 of Cheng discloses a durable chip pad comprising: a terminal metal layer 106/102 disposed on a passivating layer 108/110 and connecting to underlying chip wiring through a via through said passivating layer; an adhesion/barrier layer (116 and the CrCu portion of 118) on said terminal metal layer; a seed pad (Cu portion of 118) on said adhesion/barrier layer; a hard test barrier layer (Ni) 122 (paragraph [0014]) plated on, and enclosing, said seed pad; and a plate passivating layer (Au) 124 (paragraph [0014]) on said hard test barrier. Note that Cheng discloses layer 118 can be a multi-layered structure of Cu/CrCu (paragraph [0013]). Therefore, the Cu layer is considered to be the conducting layer pad, and the CrCu layer is considered to be part of the diffusion layer. Cheng discloses the passivating layer is formed on a semiconductor substrate (paragraph [0007]). This substrate is considered to be the IC chip. Cheng does not specifically disclose more than one pad on the chip. However, it is inherent that more than one pad is formed on the chip, since a chip with only one connection pad would be useless. Assuming, *arguendo*, Applicant can prove having more than one pad is not inherent; the claim would be obvious in view of McCormick. Figure 6 of McCormick discloses a plurality of interconnect pads formed on an IC chip. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Cheng by including more than one pad as taught by McCormick for the purpose of allowing separate electrical connections to different portions of the IC.

Art Unit: 2815

Regarding claims 9 and 10, Figure 6 of Cheng discloses said adhesion/barrier layer includes an adhesion layer (CrCu portion of 118) on barrier metallurgy (TiW) 116 (paragraph [0013]).

Claims 8 and 11-13 are rejected under 35 U.S.C. 102(e) as anticipated by Biggs or, in the alternative, under 35 U.S.C. 103(a) as obvious over Biggs in view of McCormick

Regarding claims 8 and 11-13, Figure 6 of Biggs discloses a durable chip pad on an IC chip 10, comprising: a terminal metal layer 16/18 disposed on a passivating layer 12/14 and connecting to underlying chip wiring through a via through said passivating layer; an adhesion/barrier layer 36 on said terminal metal layer; a copper seed pad 38 on said adhesion/barrier layer; a hard test barrier layer (Ni) 48 (paragraph [0012]) plated on, and enclosing, said seed pad; and a plate passivating layer (Au) 50 (paragraph [0012]) on said hard test barrier. Biggs does not specifically disclose more than one pad on the chip. However, it is inherent that more than one pad is formed on the chip, since a chip with only one connection pad would be useless. Assuming, *arguendo*, Applicant can prove having more than one pad is not inherent; the claim would be obvious in view of McCormick. Figure 6 of McCormick discloses a plurality of interconnect pads formed on an IC chip. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Biggs by including more than one pad as taught by McCormick for the purpose of allowing separate electrical connections to different portions of the IC.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng (or Cheng in view of McCormick) as applied to claim 13 above, and further in view of Homma et al. (US Pat. 6,798,050, hereinafter Homma) and Bhattacharya et al. (US PGPub 2003/0034489, hereinafter Bhatt).

Regarding claim 14, semiconductor IC chips are fabricated from a wafer of semiconductor material, and the wafer is not diced into individual chips until after the ICs have been completed. Therefore, in order to make the device of Cheng, there must have been a plurality of IC chips on a wafer at an intermediate stage of processing. However, Cheng does not explicitly disclose that the wafer is diced into individual IC chips after forming the claimed metal layers on the IC chip substrate. Figures 9A-9E of Homma discloses forming a plurality of metal layers on a wafer prior to dicing the wafer into individual chips (col. 11, lines 38-41). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Cheng by dicing the wafer after forming the claimed metal layers, thereby resulting in a plurality of ICs (with the claimed structure) on a wafer. The ordinary artisan would have been motivated to further modify Cheng in the manner described above for the purpose of simply the production process for mass production. A further difference between Cheng and the claimed invention is the ICs are identical. Bhatt discloses forming a plurality of identical ICs on a wafer (paragraph [0030]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Cheng by having a plurality of identical ICs on a wafer for the purpose of simplifying the production process for mass production of a particular IC. Note that paragraph

Art Unit: 2815

[0003] of the instant application gives a special definition to the word “die” by stating, “Each array location is known as a die and each die may harbor an IC chip”. In other words, a “die” is simply the portion of the wafer where the chip is located. Therefore, it is inherent that each of said plurality of identical ICs are located in a die on said wafer.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Biggs (or Biggs in view of McCormick) as applied to claim 13 above, and further in view of Homma and Bhatt.

Regarding claim 14, semiconductor IC chips are fabricated from a wafer of semiconductor material, and the wafer is not diced into individual chips until after the ICs have been completed. Therefore, in order to make the device of Biggs, there must have been a plurality of IC chips on a wafer at an intermediate stage of processing. However, Biggs does not explicitly disclose that the wafer is diced into individual IC chips after forming the claimed metal layers on the IC chip substrate. Figures 9A-9E of Homma discloses forming a plurality of metal layers on a wafer prior to dicing the wafer into individual chips (col. 11, lines 38-41). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Biggs by dicing the wafer after forming the claimed metal layers, thereby resulting in a plurality of ICs (with the claimed structure) on a wafer. The ordinary artisan would have been motivated to further modify Biggs in the manner described above for the purpose of simply the production process for mass production. A further difference between Biggs and the claimed invention is the ICs are identical. Bhatt discloses forming a plurality of identical ICs on a wafer (paragraph [0030]). In view of such teaching, it

Art Unit: 2815

would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Biggs by having a plurality of identical ICs on a wafer for the purpose of simplifying the production process for mass production of a particular IC. Note that paragraph [0003] of the instant application gives a special definition to the word “die” by stating, “Each array location is known as a die and each die may harbor an IC chip”. In other words, a “die” is simply the portion of the wafer where the chip is located. Therefore, it is inherent that each of said plurality of identical ICs are located in a die on said wafer.

Claims 1-5, 7-13, and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormick in view of Degani.

Regarding claims 1, 5, 7, 21 and 25, Figure 6 of McCormick discloses a chip pad comprising: a passivating layer 12; a diffusion barrier layer 16; a conducting layer pad (copper seed layer) 18 on said diffusion barrier layer; a hard test barrier (Ni) layer 26 (col. 3, lines 31-33) plated to, and enclosing, said copper seed layer pad; and a plate passivating layer (Au) (col. 3, lines 39-41) on said nickel layer. Note that it can be considered that the nickel layer 26 encloses layer 18 since it covers the only exposed surface of the layer (the upper surface). The difference between McCormick and the claimed invention is a terminal metal layer disposed on the passivating layer. Figures 1 and 9 of Degani disclose an aluminum terminal metal 13 on a passivating film 12, below a diffusion barrier layer 21/22. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the

Art Unit: 2815

invention of McCormick by including the aluminum terminal layer of Degani for the purpose of further protecting the underlying circuitry during bonding, while maintaining a low resistance contact.

Regarding claims 8 and 11-13, Figure 6 of McCormick discloses a plurality of chip pads on an IC chip 10, one or more of the chip pads being a durable pad comprising: a passivating layer 12; a diffusion barrier layer 16; a conducting layer pad (copper seed layer) 18 on said diffusion barrier layer; a hard test barrier (Ni) layer 26 (col. 3, lines 31-33) plated to, and enclosing, said copper seed layer pad; and a plate passivating layer (Au) (col. 3, lines 39-41) on said nickel layer. Note that it can be considered that the nickel layer 26 encloses layer 18 since it covers the only exposed surface of the layer (the upper surface). The difference between McCormick and the claimed invention is a terminal metal layer disposed on the passivating layer and connecting to underlying chip wiring through a via through said passivating layer. Figures 1 and 9 of Degani disclose an aluminum terminal metal 13 on a passivating film 12, below a diffusion barrier layer 21/22, wherein the terminal metal layer 13 connects to an underlying substrate through a via in the passivating layer. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of McCormick by including the aluminum terminal layer of Degani for the purpose of further protecting the underlying circuitry during bonding, while maintaining a low resistance contact.

Regarding claims 2-4, 9, 10, and 22-24, it would have been further obvious to modify McCormick by using the diffusion barrier layer 21/22 of Degani, which comprises a Ti barrier layer 21 and a CrCu adhesion layer 22 (col. 3, lines 40-50 of Degani) for the purpose of

Art Unit: 2815

providing a well known barrier material and improving adhesion between the terminal metal layer and the overlying copper seed layer.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCormick in view of Degani as applied to claim 13 above, and further in view of Homma and Bhatt.

Regarding claim 14, semiconductor IC chips are fabricated from a wafer of semiconductor material, and the wafer is not diced into individual chips until after the ICs have been completed. Therefore, in order to make the device of McCormick, there must have been a plurality of IC chips on a wafer at an intermediate stage of processing. However, McCormick does not explicitly disclose that the wafer is diced into individual IC chips after forming the claimed metal layers on the IC chip substrate. Figures 9A-9E of Homma discloses forming a plurality of metal layers on a wafer prior to dicing the wafer into individual chips (col. 11, lines 38-41). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of McCormick by dicing the wafer after forming the claimed metal layers, thereby resulting in a plurality of ICs (with the claimed structure) on a wafer. The ordinary artisan would have been motivated to further modify McCormick in the manner described above for the purpose of simply the production process for mass production. A further difference between McCormick and the claimed invention is the ICs are identical. Bhatt discloses forming a plurality of identical ICs on a wafer (paragraph [0030]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of McCormick by having a plurality of

Art Unit: 2815

identical ICs on a wafer for the purpose of simplifying the production process for mass production of a particular IC. Note that paragraph [0003] of the instant application gives a special definition to the word “die” by stating, “Each array location is known as a die and each die may harbor an IC chip”. In other words, a “die” is simply the portion of the wafer where the chip is located. Therefore, it is inherent that each of said plurality of identical ICs are located in a die on said wafer.

Response to Arguments

Applicant's arguments filed November 10, 2006 have been fully considered but they are not persuasive.

Applicant argues regarding the 102(e) rejection using Cheng and Biggs by stating “Since the present applicant was filed prior to the publication date of both applications, neither Cheng et al. nor Biggs et al. is available as a reference under 35 U.S.C. §102(e)”. Applicant has apparently misinterpreted 35 U.S.C. §102(e). When using a published application as prior art, the examiner can rely on the filing date of that application (see MPEP 706.02(f)). Since both Cheng and Biggs were filed prior to the invention of Applicant, the references can be relied upon under 35 U.S.C. §102(e).

Applicant argues regarding McCormick and Degani that McCormick does not disclose a nickel layer plated to, and enclosing, said copper seed layer pad. Although the claim has been amended, the examiner is essentially applying the same interpretation in the above rejections of claims 1, 8, and 21. Applicant states, “However, what McCormick really teaches is that layer 15

Art Unit: 2815

is only partially enclosed by the copper layer 18 and by the passivation layer 32” (it is assumed Applicant meant layer 16, not layer 15). This statement acknowledges that layer 18 at least partially encloses layer 16. The claim does not require the hard test barrier to completely surround/enclose the seed pad. In fact, the instant specification shows the hard test barrier does not completely enclose the seed layer pad, but instead merely covers the top and side surfaces. Therefore, it appears Applicant is also using a broad interpretation of the term “enclosing”. It is unclear why Applicant’s disclosed embodiment, which only partially encloses the seed layer pad, reads on the claim, but the partially enclosing hard test barrier layer of McCormick, does not read on the claim. The specification does not explicitly provide a special definition of the term “enclosing” requiring the hard test barrier to cover the top and side surfaces of the seed layer pad. Therefore, the breadth of the Examiner’s interpretation is consistent with the breadth of Applicant’s interpretation.

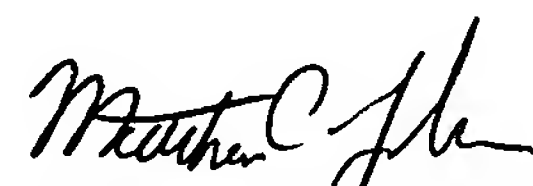
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Matthew C. Landau

January 30, 2007